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EXAMINER	
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ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,084	BUETI ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/20/04, 9/7/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not correct because the Applicants' invention is related with system and method for arbitration between processors and shared peripheral core devices in system on chip architecture (See Abstract), which is not coincided with the title "System and method for arbitration between shared peripheral core devices in system on chip architecture." A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: System and method for arbitration between processors and shared peripheral core devices in system on chip architecture.

Claim Objections

2. Claims 6, 7, 9, 16, 17, and 19 are objected to because of the following informalities:

Substitute "(SOC)" in line 3 by --SOC--, respectively.

Appropriate correction is required.

3. The claims 7 and 17 recite the subject matter "said external output path" in line 7, respectively. However, it has not been specifically clarified in the claims 7 and 17 and its intervening claims, respectively. Therefore, the Examiner presumes that the term "said external output path" could be considered as --an said external output path-- in light of the specification since it is not defined in the claims.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 9, 10, 19, and 20 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for coupling an external buffer device between external multiplexing

circuitry and peripheral core devices (See Specification, Fig. 6 and paragraph [0030]), does not reasonably provide enablement for coupling an external buffer device between external multiplexing circuitry and first and second processors (See exemplary claim 9, lines 11-13). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

The Applicants clearly describe that there are four external connections provided with the arbitration unit, actually external muxing 114, as well as an external buffer device 116 in the Specification, paragraph [0030] and Fig. 6. However, the scope of the claimed invention is that there is an external buffer device coupled between external multiplexing circuitry and external connections for each of first and second processors, which is not commensurate with the disclosure in the Specification.

Therefore, the Examiner presumes the claimed limitation "an external buffer device coupled between said external multiplexing circuitry and said external connections" could be considered as --an external buffer device coupled between said external multiplexing circuitry and an external connection-- in light of the Specification.

The claim 10 is a dependent claim of the claim 9, and the claim 20 is a dependent claim of the claim 20.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Adams et al. [US 2005/0091432 A1; hereinafter Adams].

Referring to claim 1, Adams discloses a system (i.e., System 500 in Fig. 6) for implementing arbitration between one or more shared peripheral core devices (i.e., Targets 515 of Fig. 6) in a system on chip (SOC) integrated circuit architecture (i.e., Matrix Fabric framework; See paragraph [0051]), comprising:

- a first microprocessor (i.e., CPU1 507 of Fig. 6) in communication with a first system bus (i.e., Requestor Connection Port 520 between said CPU1 and Internal Switching Fabric 550 in Fig. 6);
- a second microprocessor (i.e., CPU2 508 of Fig. 6) in communication with a second system bus (i.e., Requestor Connection Port 520 between said CPU2 and Internal Switching Fabric 550 in Fig. 6);
- at least one peripheral core device (i.e., Targets 515, e.g., External Flash Controller 503, External SDRAM Controller 504, and Internal SRAM Controller 505 in Fig. 6) accessible by both said first microprocessor and said second microprocessor (See paragraphs [0052]-[0053]); and
- an arbitration unit (i.e., Internal Switching Fabric 550 of Fig. 6) in communication with said first system bus and said second system bus (See paragraphs [0058]-[0059]);
    - wherein said arbitration unit (i.e., said Internal Switching Fabric) is configured to control communication between said at least one peripheral core device (i.e., said Targets) and said first and second microprocessors (i.e., arbitration control between CPUs and memory targets; See paragraph [0060]).

Referring to claim 2, Adams teaches a plurality of arbitration units (i.e., Arbiters in Fig. 6; actually, internal Arbiter 506 within Internal Switching Fabric 550, and external Arbiters within Targets 515 in Fig. 6), wherein

- each of said plurality of arbitration units (i.e., each of said Arbiters) is configured to control communication between said first system bus and said second system bus (i.e., Requestor

Connection Ports 520 in Fig. 6; See paragraph [0060]), and a group of peripheral core devices (i.e., Targets 515 in Fig. 6) associated therewith (i.e., Arbiter 506 associated with External Flash Controller 503, External SDRAM Controller 504 associated with its internal Arbiter, and Internal SRAM Controller 505 associated with its internal Arbiter in Fig. 6).

Referring to claim 3, Adams teaches said arbitration unit (i.e., Internal Switching Fabric 550 of Fig. 6) comprises:

- a first buffer device (i.e., Request Control Flow block 403 of Fig. 5, which is actually located within 3 Target Decoder/Router Element 502 for CPU1 507 in Fig. 6; See paragraph [0046], lines 4-6) coupled to said first system bus (i.e., Requestor Connection Port block 101 of Fig. 5; in fact, Requestor Connection Port 520 between CPU1 507 and 3 Target Decoder/Router Element 502 in Fig. 6);
- a second buffer device (i.e., Request Control Flow block 403 of Fig. 5, which is actually located within 3 Target Decoder/Router Element 502 for CPU2 508 in Fig. 6; See paragraph [0046], lines 4-6) coupled to said second system bus (i.e., Requestor Connection Port block 101 of Fig. 5; in fact, Requestor Connection Port 520 between CPU2 508 and 3 Target Decoder/Router Element 502 in Fig. 6);
- input multiplexing circuitry (i.e., Routing Logic 405 of Fig. 5) in communication with said first buffer device, said second buffer device and said at least one peripheral core device; and
- arbitration logic (i.e., Arbiter 506 of Fig. 6) in communication with said first buffer device, said second buffer device and said input multiplexing circuitry (in fact, said Arbiter being communicated with said 3 Target Decoder/Router Element, which includes said Request Control Flow blocks and said Routing Logic; See paragraph [0052]).

Referring to claim 11, Adams discloses a method (i.e., developing method for System 500 in Fig. 6; See paragraph [0003]) for implementing arbitration between one or more shared peripheral core devices (i.e., Targets 515 of Fig. 6) in a system on chip (SOC) integrated circuit architecture (i.e., Matrix Fabric framework; See paragraph [0051]), the method comprising:

- configuring a first microprocessor (i.e., CPU1 507 of Fig. 6) in communication with a first system bus (i.e., Requestor Connection Port 520 between said CPU1 and Internal Switching Fabric 550 in Fig. 6);
- configuring a second microprocessor (i.e., CPU2 508 of Fig. 6) in communication with a second system bus (i.e., Requestor Connection Port 520 between said CPU2 and Internal Switching Fabric 550 in Fig. 6);
- configuring at least one peripheral core device (i.e., Targets 515, e.g., External Flash Controller 503, External SDRAM Controller 504, and Internal SRAM Controller 505 in Fig. 6) to be accessible by both said first microprocessor and said second microprocessor (See paragraphs [0052]-[0053]); and
- configuring an arbitration unit (i.e., Internal Switching Fabric 550 of Fig. 6) in communication with said first system bus and said second system bus (See paragraphs [0058]-[0059]);
    - wherein said arbitration unit (i.e., said Internal Switching Fabric) controls communication between said at least one peripheral core device (i.e., said Targets) and said first and second microprocessors (i.e., arbitration control between CPUs and memory targets; See paragraph [0060]).

Referring to claim 12, Adams teaches

- a configuring plurality of arbitration units (i.e., Arbiters in Fig. 6; actually, internal Arbiter 506 within Internal Switching Fabric 550, and external Arbiters within Targets 515 in Fig. 6) to

control communication between said first system bus and said second system bus (i.e., Requestor Connection Ports 520 in Fig. 6; See paragraph [0060]), and a group of peripheral core devices (i.e., Targets 515 in Fig. 6) associated therewith (i.e., Arbiter 506 associated with External Flash Controller 503, External SDRAM Controller 504 associated with its internal Arbiter, and Internal SRAM Controller 505 associated with its internal Arbiter in Fig. 6).

Referring to claim 13, Adams teaches said arbitration unit (i.e., Internal Switching Fabric 550 of Fig. 6) comprises:

- a first buffer device (i.e., Request Control Flow block 403 of Fig. 5, which is actually located within 3 Target Decoder/Router Element 502 for CPU1 507 in Fig. 6; See paragraph [0046], lines 4-6) coupled to said first system bus (i.e., Requestor Connection Port block 101 of Fig. 5; in fact, Requestor Connection Port 520 between CPU1 507 and 3 Target Decoder/Router Element 502 in Fig. 6);
- a second buffer device (i.e., Request Control Flow block 403 of Fig. 5, which is actually located within 3 Target Decoder/Router Element 502 for CPU2 508 in Fig. 6; See paragraph [0046], lines 4-6) coupled to said second system bus (i.e., Requestor Connection Port block 101 of Fig. 5; in fact, Requestor Connection Port 520 between CPU2 508 and 3 Target Decoder/Router Element 502 in Fig. 6);
- input multiplexing circuitry (i.e., Routing Logic 405 of Fig. 5) in communication with said first buffer device, said second buffer device and said at least one peripheral core device; and
- arbitration logic (i.e., Arbiter 506 of Fig. 6) in communication with said first buffer device, said second buffer device and said input multiplexing circuitry (in fact, said Arbiter being communicated with said 3 Target Decoder/Router Element, which includes said Request Control Flow blocks and said Routing Logic; See paragraph [0052]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 4, 5, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams [US 2005/0091432 A1] as applied to claims 1-3 and 11-13 above, and further in view of Simcoe et al. [US 5,265,257 A; hereinafter Simcoe] and Zulian [US 5,941,967 A].

Referring to claim 4. Adams discloses all the limitations of the claim 4, except that does not expressly teach said arbitration logic is configured to detect a request for access to said at least one peripheral core device by a requesting one of said first and second microprocessors; said arbitration logic is further configured to determine the existence of a free peripheral from said at least one peripheral core device; and said arbitration logic is further configured to implement communication between a determined free peripheral and said requesting one of said first and second microprocessors; wherein said arbitration logic is further configured to inform said requesting one of said first and second microprocessors whenever no free peripheral is presently available.

Simcoe discloses a fast arbiter (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4; See Abstract and Fig. 4), wherein

- an arbitration logic (i.e., Resource Arbiter 10 of Fig. 4) is configured to detect a request for access (i.e., Request 22 of Fig. 4) to at least one peripheral core device (i.e., Resources ID=1...n 16 in Fig. 4) by a requesting one of first and second microprocessors (e.g., one of Requesters ID=1 or m in Fig. 4; See col. 6, lines 22-26, and col. 14, lines 35-38);
- said arbitration logic (i.e., said Resource Arbiter) is further configured to determine the existence of a free peripheral from said at least one peripheral core device (See col. 6, lines 26-33, and col. 14, lines 39-62); and
- said arbitration logic (i.e., said Resource Arbiter) is further configured to implement communication (i.e., coupling said Requester to said Resource) between a determined free peripheral and said requesting one of said first and second microprocessors (See col. 6, lines 33-35, and col. 15, lines 1-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration of said fast arbiter (i.e., Resource Arbiter and Access Path Controller), as disclosed by Simcoe, in said arbitration unit, as disclosed by Adams, for the advantage of providing a capability of being easily scaled to both large number of processors (i.e., requesters) and large numbers of types of peripheral core devices (i.e., resources) where there are multiple instances of each type of peripheral core device (i.e., resource; See Simcoe, col. 3, lines 3-6).

Adams, as modified by Simcoe, does not teach said arbitration logic is further configured to inform said requesting one of said first and second microprocessors whenever no free peripheral is presently available.

Zulian discloses a unit for arbitration of access to a bus of a multiprocessor system for access to a plurality of shared resources (See col. 1, lines 10-13), wherein

- an arbitration logic (i.e., arbitration unit) is configured to inform (i.e., sending RETRY signal) requesting one of first and second microprocessors (e.g., processor) whenever no free peripheral is presently available (i.e., temporarily unavailable; See col. 1, lines 21-52).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said arbitration logic (i.e., arbitration unit), as disclosed by Zulian, in said arbitration logic, as disclosed by Adams, as modified by Simcoe, so as to informing (i.e., indicating) the state of said peripheral core devices (i.e., various resources) to said first and second processors (i.e., various requesting units; See Zulian, col. 1, lines 57-62), for the advantage of freeing busses (i.e., system bus) so as to make them available for other transactions rather than keeping said busses (i.e., system bus) busy until said peripheral core device (i.e., resource) becomes free (See Zulian, col. 1, lines 53-56).

Referring to claim 5, Simcoe teaches

- said arbitration unit (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4) is configured to internally note an assignment between a free peripheral (i.e., free instance Resource) and a requesting one of said first and second microprocessors (i.e., inputting requester ID and resource ID into said Access Path Controller; See col. 15, lines 3-9).

Referring to claim 14, Adams discloses all the limitations of the claim 14, except that does not expressly teach said arbitration logic detects a request for access to said at least one peripheral core device by a requesting one of said first and second microprocessors; said arbitration logic determines the existence of a free peripheral from said at least one peripheral core device; and said arbitration logic implements communication between a determined free peripheral and said requesting one of said first and second microprocessors, informs said requesting one of said first and second microprocessors whenever no free peripheral is presently available.

Simcoe discloses an arbitration unit (i.e., a fast arbiter including Resource Arbiter 10 and Access Path Controller 20 in Fig. 4; See Abstract and Fig. 4), wherein

- an arbitration logic (i.e., Resource Arbiter 10 of Fig. 4) detects a request for access (i.e., Request 22 of Fig. 4) to at least one peripheral core device (i.e., Resources ID=1…n 16 in Fig. 4) by a requesting one of first and second microprocessors (e.g., one of Requesters ID=1 or m in Fig. 4; See col. 6, lines 22-26, and col. 14, lines 35-38);
- said arbitration logic (i.e., said Resource Arbiter) determines the existence of a free peripheral from said at least one peripheral core device (See col. 6, lines 26-33, and col. 14, lines 39-62); and
- said arbitration logic (i.e., said Resource Arbiter) implements communication (i.e., coupling said Requester to said Resource) between a determined free peripheral and said requesting one of said first and second microprocessors (See col. 6, lines 33-35, and col. 15, lines 1-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration of said arbitration unit (i.e., Resource Arbiter and Access Path Controller), as disclosed by Simcoe, in said arbitration unit, as disclosed by Adams, for the advantage of providing a capability of being easily scaled to both large number of processors (i.e., requesters) and large numbers of types of peripheral core devices (i.e., resources) where there are multiple instances of each type of peripheral core device (i.e., resource; See Simcoe, col. 3, lines 3-6).

Adams, as modified by Simcoe, does not teach said arbitration logic informs said requesting one of said first and second microprocessors whenever no free peripheral is presently available.

Zulian discloses a unit for arbitration of access to a bus of a multiprocessor system for access to a plurality of shared resources (See col. 1, lines 10-13), wherein

- an arbitration logic (i.e., arbitration unit) informs (i.e., sending RETRY signal) requesting one of first and second microprocessors (e.g., processor) whenever no free peripheral is presently available (i.e., temporarily unavailable; See col. 1, lines 21-52).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said arbitration logic (i.e., arbitration unit), as disclosed by Zulian, in said arbitration logic, as disclosed by Adams, as modified by Simcoe, so as to informing (i.e., indicating) the state of said peripheral core devices (i.e., various resources) to said first and second processors (i.e., various requesting units; See Zulian, col. 1, lines 57-62), for the advantage of freeing busses (i.e., system bus) so as to make them available for other transactions rather than keeping said busses (i.e., system bus) busy until said peripheral core device (i.e., resource) becomes free (See Zulian, col. 1, lines 53-56).

Referring to claim 15, Simcoe teaches

- said arbitration unit (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4) is configured to internally note an assignment between a free peripheral (i.e., free instance Resource) and a requesting one of said first and second microprocessors (i.e., inputting requester ID and resource ID into said Access Path Controller; See col. 15, lines 3-9).

11. Claims 6-8 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams [US 2005/0091432 A1] in view of Simcoe [US 5,265,257 A] and Zulian [US 5,941,967 A] as applied to claims 4, 5, 14, and 15 above, and further in view of Gappisch et al. [US 2003/0033490 A1; hereinafter Gappisch].

Referring to claim 6, Adams, as modified by Simcoe and Zulian, discloses all the limitations of the claim 6, including said at least one peripheral core device (e.g., External Flash Controller 503 in Fig. 6; Adams) is configured to communicate data externally from the SOC integrated circuit architecture (i.e.,

said External Flash Controller communicating with off-chip Flash memory using Matrix Fabric framework; See paragraph [0058]), except that does not teach said external communication is performed through an external output path, and said arbitration unit further comprising external multiplexing circuitry in communication with said at least one peripheral core device and said external output path.

Gappisch discloses a multiprocessor arrangements with shared non-volatile memory (See Abstract), wherein

- a peripheral device (i.e., Flash memory Array in Fig. 1) is communicating data through an external output path (i.e., Flash_DATA/Flash_ADDRESS in Fig. 1); and
- external multiplexing circuitry (i.e., multiplexer for ADDRESS/DATA_A and ADDRESS/DATA_B in Fig. 1) in communication with a peripheral core device (i.e., Access Arbitration and Wait timer in Fig. 1) and said external output path (i.e., said Flash_DATA/Flash_ADDRESS; See paragraph [0013]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said external multiplexing circuitry (i.e., multiplexer for ADDRESS/DATA_A and ADDRESS/DATA_B), as disclosed by Gappisch, in said SOC integrated circuit architecture (i.e., Matrix Fabric framework), as disclosed by Adams, as modified by Simcoe and Zulian, for the advantage of providing the improvement essentially by optimizing the synchronization between said first and second microprocessors (i.e., a plurality of microprocessors) and said at least one of peripheral core devices (i.e., one or more associated non-volatile or flash memories; See Gappisch, paragraph [0012]).

Referring to claim 7, most of the claim limitations have already been discussed/addressed with respect to claim 6, with the exception of said at least one peripheral core device being configured to communicate data to the SOC integrated circuit architecture through an external bus.

However, Adams, as modified by Simcoe, Zulian, and Gappisch further suggests that said at least one peripheral core device (i.e., said External Flash Controller 503 in Fig. 6; Adams) is configured to communicate data to the SOC integrated circuit architecture (i.e., said External Flash Controller operating a read data from off-chip Flash memory to Matrix Fabric framework; See Adams, paragraph [0058]) through an external bus (i.e., Flash_DATA/Flash_ADDRESS in Fig. 1; Gappisch).

Referring to claim 8, Simcoe teaches

- said arbitration unit (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4) is configured to internally note an assignment between a free peripheral (i.e., free instance Resource) and a requesting one of said first and second microprocessors (i.e., inputting requester ID and resource ID into said Access Path Controller; See col. 15, lines 3-9); and
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) is configured to maintain said assignment until a response is received from said free peripheral indicating a completed data transfer (See col. 6, lines 12-21 and col. 15, lines 18-26; i.e., wherein in fact that crossbar switch can be operated by the access path controller to immediately couple the particular requester to the particular resource while maintaining other couplings between different requesters and resources implies that said arbitration unit is configured to maintain said assignment until a response is received from said free peripheral indicating a completed data transfer).

Referring to claim 16, Adams, as modified by Simcoe and Zulian, discloses all the limitations of the claim 16, including said at least one peripheral core device (e.g., External Flash Controller 503 in Fig. 6; Adams) communicates data externally from the SOC integrated circuit architecture (i.e., said External Flash Controller communicating with off-chip Flash memory using Matrix Fabric framework; See

paragraph [0058]), except that does not teach said external communication is performed through an external output path, and said arbitration unit further includes external multiplexing circuitry in communication with said at least one peripheral core device and said external output path.

Gappisch discloses a multiprocessor arrangements with shared non-volatile memory (See Abstract), wherein

- a peripheral device (i.e., Flash memory Array in Fig. 1) is communicating data through an external output path (i.e., Flash_DATA/Flash_ADDRESS in Fig. 1); and
- external multiplexing circuitry (i.e., multiplexer for ADDRESS/DATA_A and ADDRESS/DATA_B in Fig. 1) in communication with a peripheral core device (i.e., Access Arbitration and Wait timer in Fig. 1) and said external output path (i.e., said Flash_DATA/Flash_ADDRESS; See paragraph [0013]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said external multiplexing circuitry (i.e., multiplexer for ADDRESS/DATA_A and ADDRESS/DATA_B), as disclosed by Gappisch, in said SOC integrated circuit architecture (i.e., Matrix Fabric framework), as disclosed by Adams, as modified by Simcoe and Zulian, for the advantage of providing the improvement essentially by optimizing the synchronization between said first and second microprocessors (i.e., a plurality of microprocessors) and said at least one of peripheral core devices (i.e., one or more associated non-volatile or flash memories; See Gappisch, paragraph [0012]).

Referring to claim 17, most of the claim limitations have already been discussed/addressed with respect to claim 16, with the exception of said at least one peripheral core device being configured to communicate data to the SOC integrated circuit architecture through an external bus.

However, Adams, as modified by Simcoe, Zulian, and Gappisch further suggests that said at least one peripheral core device (i.e., said External Flash Controller 503 in Fig. 6; Adams) is configured to

communicate data to the SOC integrated circuit architecture (i.e., said External Flash Controller operating a read data from off-chip Flash memory to Matrix Fabric framework; See Adams, paragraph [0058]) through an external bus (i.e., Flash_DATA/Flash_ADDRESS in Fig. 1; Gappisch).

Referring to claim 18, Simcoe teaches

- said arbitration unit (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4) internally notes an assignment between a free peripheral (i.e., free instance Resource) and a requesting one of said first and second microprocessors (i.e., inputting requester ID and resource ID into said Access Path Controller; See col. 15, lines 3-9); and
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) maintains said assignment until a response is received from said free peripheral indicating a completed data transfer (See col. 6, lines 12-21 and col. 15, lines 18-26; i.e., wherein in fact that crossbar switch can be operated by the access path controller to immediately couple the particular requester to the particular resource while maintaining other couplings between different requesters and resources implies that said arbitration unit is configured to maintain said assignment until a response is received from said free peripheral indicating a completed data transfer).

12. Claims 9, 10, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams [US 2005/0091432 A1] in view of Simcoe [US 5,265,257 A] and Zulian [US 5,941,967 A] as applied to claims 4, 5, 14, and 15 above, and further in view of Gappisch [US 2003/0033490 A1] and Potter, JR. [US 2004/0187112 A1; hereinafter Potter].

Referring to claim 9, Adams, as modified by Simcoe and Zulian, discloses all the limitations of the claim 9, including said at least one peripheral core device (e.g., External Flash Controller 503 in Fig. 6; Adams) is configured to communicate data to and from (e.g., data read/write operation) the SOC

integrated circuit architecture (i.e., said External Flash Controller communicating with off-chip Flash memory using Matrix Fabric framework; See paragraph [0058]), except that does not teach said communication is performed through an associated external connection for each of said first and second microprocessors, and said arbitration unit further comprising external multiplexing circuitry in communication with said at least one peripheral core device and said external connections; and said arbitration unit further comprising an external buffer device coupled between said external multiplexing circuitry and an external connection.

Gappisch discloses a multiprocessor arrangements with shared non-volatile memory (See Abstract), wherein

- a peripheral device (i.e., Flash Memory Array in Fig. 1) is communicating data through an associated external connection for each of said first and second microprocessors (i.e., ADDRESS/DATA_A and ADDRESS/DATA_B in Fig. 1); and
- external multiplexing circuitry (i.e., multiplexer for said ADDRESS/DATA_A and ADDRESS/DATA_B in Fig. 1) in communication with a peripheral core device (i.e., Access Arbitration and Wait timer in Fig. 1) and said external connections (i.e., said ADDRESS/DATA_A and ADDRESS/DATA_B; See paragraph [0013]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said external multiplexing circuitry (i.e., multiplexer for ADDRESS/DATA_A and ADDRESS/DATA_B), as disclosed by Gappisch, in said SOC integrated circuit architecture (i.e., Matrix Fabric framework), as disclosed by Adams, as modified by Simcoe and Zulian, for the advantage of providing the improvement essentially by optimizing the synchronization between said first and second microprocessors (i.e., a plurality of microprocessors) and said at least one of peripheral core devices (i.e., one or more associated non-volatile or flash memories; See Gappisch, paragraph [0012]).

Adams, as modified by Simcoe, Zulian and Gappisch, does not teach said arbitration unit comprising an external buffer device coupled between said external multiplexing circuitry and an external connection.

Potter discloses a system for dynamic ordering in a network processor (See Abstract), wherein

- an arbitration unit (i.e., Router/Switch 200 of Fig. 1) comprising an external buffer device (i.e., buffer and queuing unit 210 of Fig. 2) coupled between an external multiplexing circuitry (i.e., Selector Circuit 250 of Fig. 2) and an external connection (i.e., external connection 290 coupling external memory resources 280 in Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said dynamic ordering using said external buffer device (i.e., buffer and queuing unit and its control), as disclosed by Potter, in said arbitration unit, as disclosed by Adams, as modified by Simcoe, Zulian and Gappisch, for the advantage of maintaining a proper order among a plurality of data operations in said system (i.e., threads in a multi-threaded processing system; See Potter, paragraph [0011]).

Referring to claim 10, Simcoe teaches

- said arbitration unit (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4) is configured to receive incoming data from one of said external connections (i.e., said Resource Arbiter receiving Resource Type 24 from one of Requesters ID=1…m in Fig. 4) and identify a target destination (i.e., Resource ID) for said incoming data (See col. 6, lines 36-51);
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) is configured to internally note an assignment between a free peripheral (i.e., free instance Resource) and said target destination (i.e., inputting requester ID and resource ID into said Access Path Controller; See col. 15, lines 3-9); and

said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) is configured to maintain said assignment until the completion of a completed data transfer between said one of said external connections (i.e., one of Requesters ID=1...m) and said target destination (i.e., Resource), through said free peripheral (See col. 6, lines 12-21 and col. 15, lines 18-26; i.e., wherein in fact that crossbar switch can be operated by the access path controller to immediately couple the particular requester to the particular resource while maintaining other couplings between different requesters and resources implies that said arbitration unit is configured to maintain said assignment until the completion of a completed data transfer between said one of said external connections and said target destination, through said free peripheral, free instance device).

Referring to claim 19, Adams, as modified by Simcoe and Zulian, discloses all the limitations of the claim 19, including said at least one peripheral core device (e.g., External Flash Controller 503 in Fig. 6; Adams) communicates data to and from (e.g., data read/write operation) the SOC integrated circuit architecture (i.e., said External Flash Controller communicating with off-chip Flash memory using Matrix Fabric framework; See paragraph [0058]), except that does not teach said communication is performed through an associated external connection for each of said first and second microprocessors, and said arbitration unit further includes external multiplexing circuitry in communication with said at least one peripheral core device and said external connections; and said arbitration unit further includes an external buffer device coupled between said external multiplexing circuitry and an external connection.

Gappisch discloses a multiprocessor arrangements with shared non-volatile memory (See Abstract), wherein

- a peripheral device (i.e., Flash Memory Array in Fig. 1) is communicating data through an associated external connection for each of said first and second microprocessors (i.e., ADDRESS/DATA_A and ADDRESS/DATA_B in Fig. 1); and

- external multiplexing circuitry (i.e., multiplexer for said ADDRESS/DATA_A and ADDRESS/DATA_B in Fig. 1) in communication with a peripheral core device (i.e., Access Arbitration and Wait timer in Fig. 1) and said external connections (i.e., said ADDRESS/DATA_A and ADDRESS/DATA_B; See paragraph [0013]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said external multiplexing circuitry (i.e., multiplexer for ADDRESS/DATA_A and ADDRESS/DATA_B), as disclosed by Gappisch, in said SOC integrated circuit architecture (i.e., Matrix Fabric framework), as disclosed by Adams, as modified by Simcoe and Zulian, for the advantage of providing the improvement essentially by optimizing the synchronization between said first and second microprocessors (i.e., a plurality of microprocessors) and said at least one of peripheral core devices (i.e., one or more associated non-volatile or flash memories; See Gappisch, paragraph [0012]).

Adams, as modified by Simcoe, Zulian and Gappisch, does not teach said arbitration unit including an external buffer device coupled between said external multiplexing circuitry and an external connection.

Potter discloses a method for dynamic ordering in a network processor (See Abstract), wherein

- an arbitration unit (i.e., Router/Switch 200 of Fig. 1) including an external buffer device (i.e., buffer and queuing unit 210 of Fig. 2) coupled between an external multiplexing circuitry (i.e., Selector Circuit 250 of Fig. 2) and an external connection (i.e., external connection 290 coupling external memory resources 280 in Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said dynamic ordering using said external buffer device (i.e., buffer and queuing unit and its control), as disclosed by Potter, in said arbitration unit, as disclosed by Adams, as modified by Simcoe, Zulian and Gappisch, for the advantage of maintaining a proper order among a plurality of data operations in said system (i.e., threads in a multi-threaded processing system; See Potter, paragraph [0011]).

Referring to claim 20, Simcoe teaches

- said arbitration unit (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4) receives incoming data from one of said external connections (i.e., said Resource Arbiter receiving Resource Type 24 from one of Requesters ID=1…m in Fig. 4) and identifies a target destination (i.e., Resource ID) for said incoming data (See col. 6, lines 36-51);
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) internally notes an assignment between a free peripheral (i.e., free instance Resource) and said target destination (i.e., inputting requester ID and resource ID into said Access Path Controller; See col. 15, lines 3-9); and
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) maintains said assignment until the completion of a completed data transfer between said one of said external connections (i.e., one of Requesters ID=1…m) and said target destination (i.e., Resource), through said free peripheral (See col. 6, lines 12-21 and col. 15, lines 18-26; i.e., wherein in fact that crossbar switch can be operated by the access path controller to immediately couple the particular requester to the particular resource while maintaining other couplings between different requesters and resources implies that said arbitration unit maintains said assignment until the completion of a completed data transfer between said one of said external connections and said target destination, through said free peripheral, free instance device).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wicki et al. [US 5,892,766 A] disclose method and apparatus for coordinating access to an output of a routing device in a packet switching network.

Hofmann et al. [US 6,823,411 B2] disclose N-way pseudo cross-bar having an arbitration feature using discrete processor local busses.

Weber et al. [US 2005/0076125 A1] disclose low power shared link arbitration.

Kim [US 2004/0041813 A1] discloses system on-a-chip processor for multimedia.

Crews et al. [US 5,619,661 A] disclose dynamic arbitration system and method.

Harral [US 6,978,329 B1] discloses programmable array-based bus arbiter.

Walsh [US 4,641,266] discloses access-arbitration scheme.

Tseng et al. [US 2004/0068625 A1] disclose multiple-grant controller with parallel arbitration mechanism and related method.

Eberle et al. [US 2003/0156597 A1] disclose method and apparatus for speculative arbitration.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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